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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,848	12/02/2003	Diane C. Boyd	YOR920030335US1 (16900)	3237

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EXAMINER	
GEORGE, PATRICIA ANN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,848	BOYD ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/18/2006 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-2, 4-5, 7-8, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al. of US 6,486,037 in view of Sugihara et al. of US 6,566,734, Hsu in US 5,468,657, and Park (6,064,092).

As for claim 1, see figures 5a-c, where Norcott et al. disclosed the process of making a buried oxide region utilizing a low dose oxygen implant step (ab.) (commonly

known as SIMOX) providing: a SOI substrate having an SOI layer located on a buried insulating layer (col.4, l.48); forming a block mask having a channel via atop said SOI substrate (col.4, l.30-35); a self-aligned, localized oxide region (col.4, l.47) in SOI layer on top of said buried insulating layer which forms a thinned portion of said SOI layer (col.6, l.12-13); and removing block mask (col.7, l.65-67).

As for claim 2, Norcott et al. disclosed implanting oxygen dopant via a patterned channel to dope a portion of said SOI layer (col.4, l.66-67); and annealing the substrate to convert the doped region into an oxide region that is on top of and in contact with a buried insulating layer providing a thin portion of the SOI layer (col.6, l.35-46).

As for claim 4, Norcott et al. disclosed the SOI layer comprises isolation regions in figure 5c.

As for claim 5, Norcott et al. disclosed an oxygen dopant is implanted with a dose of about 1×10^{17} cm^{-2} or above (col.2, l. 60-61).

As for claim 7, Norcott et al. disclosed an oxygen dopant is implanted having a current beam density ranging from about 0.5 to 500 mA cm2 which encompasses the claimed range of 5.0 mA cm.sup.-2 to about 10.0 mA cm.sup.-2. See column10, lines 61-62.

As for claim 8, Norcott et al. disclosed an SOI layer comprises Si, SiGe, SiGeC, SiC or combinations thereof (col.4, l.40-45).

Norcott et al. failed to openly disclose the claimed limitations toward methods of forming: (1) source/drain extensions in regions doped with IIIA or V dopants (col.11, l.35-40); and (2) gate in via channel, as in claims 1, 12, 20, 24, and 26. Norcott et al.

failed to disclose: (1) forming a block mask having a channel via atop said SOI substrate; forming a gate in said channel via; removing at least said block mask (as in claim 1); forming a dummy gate region atop said material stack; forming a masking layer substantially coplanar with a top surface of said dummy gate region; removing said dummy gate region to produce said block mask having said channel via; and forming a conformal film atop said block mask and within said channel via (as in claim 12); etching horizontal surfaces of said conformal film and said material stack to expose said SOI layer; forming a gate conductor atop said gate dielectric and removing said block mask (as in claim 20); gate conductor material is polysilicon (as in claim 24); and (2) forming source/drain extensions (as in claim 1), with a thickness of about 20.0 nm to about 70.0 nm (as in claim 26).

However, Norcott did teach SOI devices and circuits, such as microprocessors, memory cells, advanced integrated circuits, and even more complicated circuits (col.8, l.14-20), which all contain said structures (1 and 2).

Sugihara et al. teaches well known, conventional methods of forming a field effect transistor (FET), including: (1) the forming of source/drain extension regions (ab.), as in claim 1: doped with arsenic or phosphorous, from the claimed groups of IIIA or V dopants (col.11, l.35-40), as in claim 26; and (2) the forming of gate (ab.) in via channel, as in claim 1: forming a dummy gate region (ab.) on a material stack (fig.2); forming a masking layer, coplanar to the gate (col.8, l1-4); removing the dummy gate (col.8, l.61-62) to produce said block mask (col.8, l.64-65); and forming a conformal film over and within the channel (fig. 3 or 6), as in claim 12. Also see figures 14 then 15, which shows

sequential steps of forming gate electrode by forming a gate dummy followed by the block mask method and, as in claim 12. Further, Sugihara also teaches forming the gate in the channel provides: etching horizontal surfaces of said conformal film and the material stack to expose said SOI layer (see figure 8); forming a gate dielectric atop said SOI layer (col.9, l55 and figure 12, 17); forming a gate conductor atop said gate dielectric (col.9, l.54-55), as in claims 20 and 24.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the structural methods of forming conventional, commonly used semiconductor source/drain extension regions, and gates, as Sugihara, after making a SIMOX substrate for semiconductor devices, as Norcott, because the methods are well known and conventional.

Norcott does not teach the localized oxide region being in contact with an upper surface of the buried insulating layer.

Hsu also teaches a process improvement to the well known SIMOX process of making a buried oxide regions providing a localized oxide region (fig. 1B, 30) that is in contact with an upper surface of the buried insulating layer (fig. 1C, 44 and see discussion in col.4, lines 35-60).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to select a structure where the localized oxide region that is in contact with an upper surface of the buried insulating layer, as Hsu, when forming a

localized oxide region, as Norcott, because Hsu teaches a known structure used when forming localized oxide regions that is effective when forming MOSFET devices.

The modified teaching of Norcott, fails to teach the localized oxide region thins a portion of the SOI layer to a second thickness that is less than a first thickness and does not extend entirely across the buried insulating layer.

Park teaches, in figures 3D-3F, a channel region located in silicon (40) on insulating layer (60) (note first thickness in figure 3D) of a silicon on insulating substrate including channel region (73) (note area under 73 in figure 3F, as second thickness) being thinned by presence of an underlying localized oxide region (60a) on top of and in contact with buried insulating layer (60). Park teaches the third LOCOS area acts as the channel region and because the channel region is thin, low junction capacitance can be achieved along with the provision of this oxidation blocking layer that allows dopants to be added to form low resistance source and drain regions on opposite sides of the thin region which acts as the channel region (see abstract).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include localized oxide region thins a portion of the SOI layer to a second thickness that is less than a first thickness and does not extend entirely across the buried insulating layer, as Park, when forming the thin channel MOSFET, as Norcott, because Park teaches a method that results in improvements such as thinner channel region provides low junction capacitance, and an oxidation blocking layer which provides an improvement to the S/D regions as well.

Claim Rejections - 35 USC § 103

Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al., Sugihara et al., Hsu, and Park, as applied to claims 1-2, 4-5, 7-8, and 26 above, further in view of Dolan et al. of US 6,417,078.

The combined reference of Norcott fails to teach the following properties of the SOI region: the thickness of the SOI layer 20.0 nm to about 70.0 nm, as in claim 3; and the thinning of a portion of the region, as in claim 9.

Dolan teaches a process improvement to SIMOX, comprising a range of SOI layer thickness from about 10 to 250 nm (ab.) which encompasses the claimed range of 20.0 nm to about 70.0 nm, as in claim 3.

Dolan also teaches the localized oxide region thins a portion of the SOI layer to 30 to 300 nm (col.3, l.65-67), which encompasses the claimed range of less than about 50.0 nm, as in claim 9.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to select the thicknesses of the SOI region, both SOI layer and localized oxide region, in the modified method of Norcott et al., because the reference of Dolan teaches such thicknesses are desirable for a process improvement which enhances the performance of devices manufactures on SOI structures.

Claim Rejections - 35 USC § 103

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al., Sugihara et al., Hsu, and Park, as applied to claims 1-2, 4-5, 7-8, and 26 above, further in view of Suguro et al. of US 6,465,290.

The combined reference of Norcott fails to teach source/drain extension regions having a thickness of about 20.0 nm to about 70.0 nm.

Suguro et al. teaches a process improvement of source/drain extension regions having a thickness of about 20.0 nm to about 70.0 nm (col.18, l.57-61), as in claim 27.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the process improvement, of Suguro, when forming a semiconductor, as above, because it is a cost savings to improve the process.

Claim Rejections - 35 USC § 103

Claims 10-12, 20, and 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al., Sugihara et al., Hsu, and Park, as applied to claims 1-2, 4-5, 7-8, and 26 above, further in view of Yiu et al. of US 2003/0186511.

The combined reference of Norcott et al. disclosed forming a material stack on a SOI substrate prior to forming a block mask (see fig. 5a-c), as in claim 10., 12, 20, and 24

The combined reference of Norcott et al. failed to disclose including a pad oxide layer positioned on the SOI layer, and a silicon nitride (Si3N4) etch stop layer positioned on the pad oxide layer.

Yiu teaches a conventional layering technique used over the isolation area includes: a pad oxide layer positioned on the SOI layer, and a silicon nitride (Si3N4) etch stop layer positioned on the pad oxide layer (para. 1-11), as in claims 10 –12, 20 and 24.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include subsequent layers when forming a field effect transistor with SIMOX, as combined by Norcott et al. and Sugihara, because Yiu teaches it is known and conventional.

Claim Rejections - 35 USC § 103

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al., Sugihara et al., Hsu, Park, and Yiu et al., as applied to claims 10-12, 20, and 24 above, further in view of Miyakawa et al. of US 6,162,677.

Norcott was silent as to the limitations of silicon nitride in claims 14.

Miyakawa et al. teaches known and industry used methods for silicon nitride etch stop (col.8, l.56) formed by a CVD process (col.8, l.60), having a thickness of 50 nm (col.8, l.54-65) within the claimed ranging from about 50.0 nm to about 150.0 nm, as in claims 14.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the SiN methods of Miyakawa, when forming a semiconductor, as above, because Miyakawa methods are known and used.

Claim Rejections - 35 USC § 103

Claims 15, and 21 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al., Sugihara et al., Hsu, Park, and Yiu et al., as applied in claims 10-12, 20, and 24 above, further in view of Miyakawa et al. of US 6,162,677 (as applied to claim 14 above), and Adkisson et al of US US 2002/0153587.

The combined teachings of Norcott illustrates the gate conductor is formed over the gate mask and dielectric, and planarizing until the gate conductor material is coplanar with the block mask (see figure 12), as in claim 22.

The combined reference of Norcott teaches forming a conformal film over and within the channel (fig. 3 or 6), as in claim 15, but fail to teach the conventional limitations of claims 15, and 21-23.

Adkisson teaches widely known conventional semiconductor fabrication techniques, such as: etching of regions of a layer not underlying said patterned photoresist, as in claim 15 (figure 3A, and para 52); the forming of a gate dielectric by thermal oxidation (para. 53), as in claims 21 and 22; etching silicon nitride selective to pad oxide layer, as in claim 23 (para. 70, l.6); and etching pad oxide layer with a RIE comprising HF and NH.sub.3, as in claim 23 (para. 66).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to use the conventional limitations of thermal oxidation, selective etching, and RIE chemistry, of Adkisson et al., when forming the combined

semiconductor invention, above, because it is obvious to use such widely known conventional techniques.

Claim Rejections - 35 USC § 103

Claims 16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al., Sugihara et al., Hsu, Park, Yiu et al., (as applied to claims 10-12, 20, and 24 above), Miyakawa et al., and Adkisson et al. (as applied to claim 15 above) further in view of Tan of US 6,001,706.

The combined reference of Norcott is silent as to polysilicon etch, including plasma etch with HBr, or wet etch with KOH chemistries.

Tan et al. teaches conventionally used methods for polysilicon etch, including plasma etches with HBr, or wet etch with KOH chemistries, as in claims 16, 18, and 19.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the conventionally used polysilicon etches, of Tan, when forming a semiconductor, as above, because they are conventional.

Claim Rejections - 35 USC § 103

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al., Sugihara et al., Hsu, Park, and Yiu et al., Miyakawa et al. of US 6,162,677, and Adkisson et al of US US 2002/0153587, further in view of Graas of USPN 5,360,995.

The combined reference of Notrcott is silent as to removal of photo resist using an O.sub.2 ash process.

Graas teaches the widely used, known, common method for removal of photo resists using an O.sub.2 ash process, as in claim 17 (col. 5-6, l. 67-1), as in claim 17.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the conventionally ash for polysilicon, of Graas, when forming a semiconductor, as above, because it is a widely used, known, common method.

Claim Rejections - 35 USC § 103

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al., Sugihara et al., Hsu, Park, and Yiu et al., as applied to claims 10-12, 20, and 24 above, further in view of Lim et al. of US 6,673, 695.

The combined reference of Norcott is silent as to method of HD deposition of an oxide mask layer.

As for claim 13, Lim et al. teaches the widely available method of HD deposition of an oxide mask layer (col. 5, l.40), as in claims 13.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to use the method of HD, of Lim, to deposit the oxide mask, when forming a semiconductor, as above, because use of HDP for an oxide mask is widely available.

Claim Rejections - 35 USC § 103

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Norcott et al., Sugihara et al., Hsu, Park, and Yiu et al., as applied to claims 10-12, 20, and 24 above, further in view of Yang et al. of US 6,110,779.

The combined reference of Norcott is silent as to doping the polysilicon prior to removing a hard mask.

Yang teaches a conventional method for doping polysilicon with use of a hard mask, which is written on prior to removing a hard mask. (col.4, l. 6-8), as in claim 25.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the conventional method of doping polysilicon, of Yang, when forming a semiconductor, as above, because the method is conventional.

Response to Arguments

Applicants' arguments/~~abandonments~~ amendments filed 01/06/06 pertaining to a localized oxide region iin a SOI layer on top of, and in contact with, an upper surface of a buried insulating layer distinguish over the previous rejection over ref Norcott et al. of US 6,486,037 in view of Sugihara et al. of US 6,566,734. A modified rejection appears above to address applicants' newly submitted amendments.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is

(571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000

Patricia A George
Examiner
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PAG
08/06

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